3D IC Inter-Die Test Implementation Using IEEE1838

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1. Motivation

- 3D IC DFT methodology is one of important item to hedge risks in 3D IC
- Since inter-die test is new requirement only for 3D IC, it is most important item in 3D IC DFT methodology
- Even though 3D IC inter-die test is new technology, it has not been evaluated yet in real design
- 3D IC inter-die test methodology is proposed and implemented in real design
  - IEEE1838 is adopted for 3D IC inter-die test and it is also evaluated to check its functionality
  - To check connectivity of signals between specific locations, wrapper cell is inserted at specified position
  - Test pattern utilizing the die wrapper register (DWR), is generated for 3D IC inter-die test
  - Above 3D IC inter-die test methodology items are implemented on real design and 3D IC inter-die test functionality is also verified using simulation

2. DWR Insertion Scheme

- In IEEE1838, die wrapper register (DWR) pair is used to conduct 3D IC inter-die test
- To insert DWR at specific location, wrapper cell generated by synthesis tool is used
  - It is required to insert DWR at specific location in real design to support hierarchical flow
  - Synthesis tool can add wrapper cells at specified location which can be used as DWR in the inter-die test
- The DWR configuration information is delivered to die level design for inter-die test mode
  - Test model file is delivered to upper level design to deliver the scan test mode information of lower level

```
set_boundary_cell -class core_wrapper -type WC_D1 -internal_pins { \
BLK_DWR/instace0/Y \
BLK_DWR/instace1/Y \
BLK_DWR/instace2/Y \
BLK_DWR/instace3/Y \
BLK_DWR/instace4/Y \
BLK_DWR/instace5/Y \
BLK_DWR/instace6/Y \
BLK_DWR/instace7/Y \
}
```

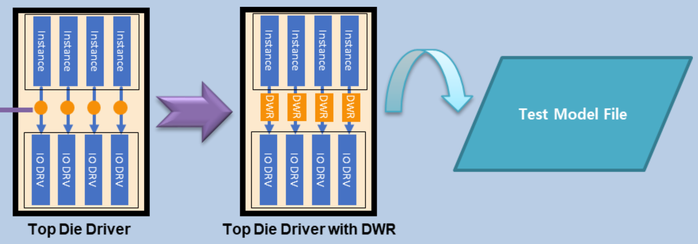

Figure1 DWR location specification to generate DWR inserted design and test model

3. IEEE1838 Implementation

- IEEE1838 test access component is inserted and inter-die test mode is defined at each die
  - IEEE1838 test access component mainly consists of PTAP, STAP, and DWR
  - At bottom die, PTAP, STAP, and DWR are integrated in RTL design and inter-die test mode is defined
  - At top die, PTAP and DWR are integrated in RTL design and inter-die test mode is also defined
- Virtual stacked die design is prepared to generate virtual test procedure file
  - Two dies are instantiated in virtual stacked die and inter-die signals are connected corresponding pins
  - Inter-die test mode is defined again and test procedure file is generated for virtual stacked die design

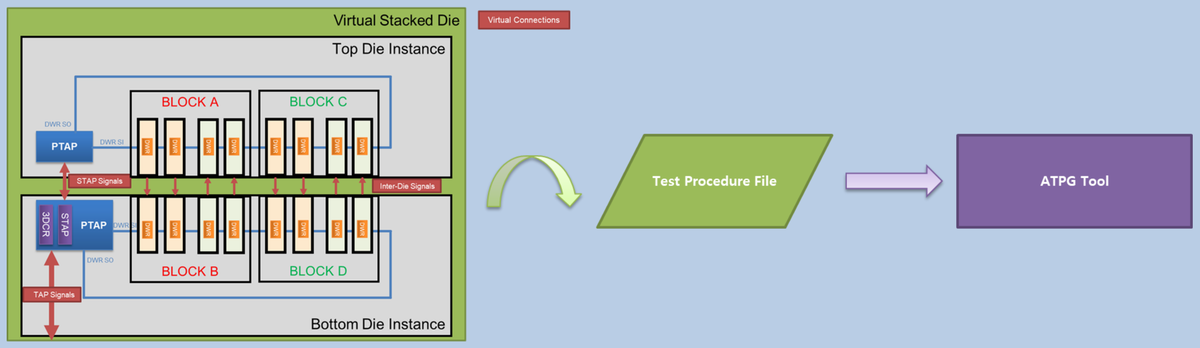

Figure2 Virtual stacked die test procedure file generation to use it in ATPG

4. Inter-Die Test Pattern Generation

- Virtual stacked die design is used to generate inter-die test pattern
  - For virtual stacked die design, inter-die test mode is defined in previous step
  - Test procedure file for inter-die test mode is delivered to ATPG tool
- Inter-die signals are added as faults during ATPG for inter-die test
  - Inter-die signals are connected corresponding pins between two dies in the virtual stacked die
  - Signals connected to both dies are the targets of the inter-die test to check connectivity of signals
  - At each die, Inter-die signal pins are added as faults in the ATPG
- ATPG and verification using simulation is done successfully
  - Inter-die test patterns are generated successfully in ATPG with 100% test coverage
  - Generated inter-die test patterns are verified using simulation and it could detect faults correctly

```
----------------------------------------------------
    Uncollapsed Stuck Fault Summary Report
----------------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT       8640
  detected_by_simulation         DS       (8640)
Possibly detected                PT          0
Undetectable                     UD          0
ATPG untestable                  AU          0
Not detected                     ND          0
----------------------------------------------------
total faults                               8640
test coverage                            100.00%
fault coverage                           100.00%
----------------------------------------------------
```

```
TEST COMPLETED WITH NO COMPARISON ERRORS

Fail Report on DO[10]:
   Logic 0 checks(failures) =      28001(          0), Logic 1 checks(failures) =      28211(          0)
Fail Report on DO[11]:
   Logic 0 checks(failures) =          0(          0), Logic 1 checks(failures) =         13(          0)
Fail Report on DO[0]:
   Logic 0 checks(failures) =         25(          0), Logic 1 checks(failures) =         14(          0)
Fail Report on DO[1]:
   Logic 0 checks(failures) =         27(          0), Logic 1 checks(failures) =         12(          0)
Fail Report on DO[2]:
   Logic 0 checks(failures) =         18(          0), Logic 1 checks(failures) =         21(          0)
Fail Report on DO[3]:
   Logic 0 checks(failures) =          9(          0), Logic 1 checks(failures) =         30(          0)
```

Figure3 ATPG result of inter-die test

5. Summary

- 3D IC inter-die test methodology is one of hot topic in 3D IC technology
  - Many design companies are considering adopting 3D IC packaging to obtain merits of 3D IC
  - 3D IC DFT methodology should be prepared to hedge the risk of 3D IC
  - Since Inter-die test is new requirement only for 3D IC, it is most important item in 3D IC DFT methodology
- To insert DWR to specific location, wrapper cell integration flow is used
  - DWR is inserted to specified location using synthesis tool and DWR information is also generated
- IEEE1838 is adopted and evaluated in real 3D IC design
  - PTAP, STAP, and DWR of IEEE1838 are evaluated in real design
  - Their connections and functionality is also evaluated in real design
- To generate inter-die test pattern, virtual stacked die design is prepared and used
  - In virtual stacked design, inter-die test mode is defined and test procedure file is generated for ATPG
  - Inter-die signals are connected corresponding pins for both dies and they are set to target faults in ATPG
- Generated inter-die test pattern could detect faults effectively
  - Inter-die test pattern which provides 100% test coverage is generated successfully for virtual stacked die
  - The test pattern operates correctly in simulation and it could detect faults on inter-die signal